



ALPHA DATA

XRM2-ADC-Q8/250 User Manual

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1 Introduction

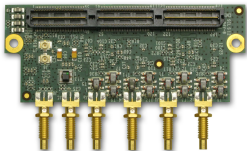


Figure 1 : XRM2-ADC-Q8/250


The XRM2-ADC-Q8-250 is a front panel adapter card designed for use with Alpha Data's PMC cards using Virtex 4, Virtex5 and Virtex6 FPGAs.

The XRM2-ADC-Q8-250 provides four ac-coupled channels of analogue to digital conversion with 14 bit resolution and supports sampling rates up to 250 MHz . It is aimed at applications such as IF Signal Sampling.

An external clock source may be used or an internally generated clock can be used to provide the sampling clock. The sampling clock can use the external clock input directly or pre-scaled, allowing the use of a high frequency source.

One auxiliary I/O port is provided for use as a trigger input/ general purpose signalling. A further pair of ports are provided for inter-board connection, fast triggering etc.

EMI

 This equipment generates, uses and can radiate electromagnetic energy. It may cause or be susceptible to electromagnetic interference if not installed and used with adequate EMI protection for specific applications


2 Installation

The XRM-ADC-Q8-250 is designed to plug in to the front panel connector (SAMTEC QSH series) on an Alpha-Data PMC card. The retaining screws should be tightened to secure the XRM-ADC-Q8-250.

Note:

This operation should not be performed while the PMC card is powered up.

2.1 Handling instructions

 Observe precautions for preventing damage to components by electrostatic discharge. Personnel handling the board should take SSD precautions. Avoid flexing the board.

3 Specification

3.1 Inputs

3.1.1 Connector type

SSMC

3.1.2 IA Signal (J1), IB Signal (J2)

| | |
|----------------|-------------------------------------|
| Input: | 0 Ohms |
| Bandwidth: | 4.5 MHz to 1000 MHz (3 dB) |
| Nominal Level: | +10 dBm (2.0 Vppk = ADC full scale) |
| SFDR: | >60 dBc ^[1] |

3.1.3 QA Signal (J3), QB Signal (J4)

| | |
|----------------|-------------------------------------|
| Input: | 50 Ohms |
| Bandwidth: | 4.5 MHz to 1000 MHz (3 dB) |
| Nominal Level: | +10 dBm (2.0 Vppk = ADC full scale) |
| SFDR: | >60 dBc ^[2] |

3.1.4 Clock In (J5)

| | |
|-------------------------|---|
| Input: | 50 Ohms |
| Nominal Level: | 0 dBm nominal (640 mV pk to pk) +12 dBm maximum (2.5 V pk to pk) |
| Frequency: | 1600MHz abs max. |
| Supported sample rates: | 40 MHz to 250 MHz |

[1] - Measured using internal oscillator, signal source -8 dBm at 40 MHz, 250 MHz sampling.

[2] - Measured using internal oscillator, signal source -8 dBm at 40 MHz, 250 MHz sampling

3.2 Input /Output

3.2.1 Trig IO Port (J8)

Buffered, user configurable as input or output.

Input: 4k7 Ohms
Level: +3V3 LVTTTL

3.2.2 Aux. Ports (J6,J7)

Unbuffered, configurable as input or output

Input: dc coupled
Level: +2v5 LVTTTL

Note: these pins are connected directly to the FPGA and should be used with caution.

4 Options

4.1 Order Codes

Virtex4, Virtex5

XRM-ADC-Q8-250

Virtex6, Virtex7, Kintex7

XRM2-ADC-Q8-250

Please check [the Alpha Data Website](#)  for the current valid order codes.

5 Related Documents

ADM-XRC4SX/LX User Manuals

ADM-XRC4FX User Manual

ADPE-4FX User Manual

ADM-XRC5LX User Manual

ADM-XRC5T1 User Manual

ADM-XRC5T2 User Manual

ADM-XRC6T1 User Manual

ADM-XRC6GE User Manual

ADM-XRC6TL User Manual

ADM-XRC6TL User Manual

ADM-XRC7K1 User Manual

ADM-XRC7V1 User Manual

6 Design Examples

Example UCF, HDL files and Application software are available from Alpha Data for purchasers of this card.

Please note that export licence restrictions apply to both the hardware and also the example code.

For customers in the EU, these example files are classified as supporting the use of dual-use items and are subject to controls if exported from the community but are freely available for use within EU countries.

For customers in Australia, Canada, Japan, New Zealand, Norway, Switzerland or the USA these files are classified as supporting the use of dual-use items and are exported under the Open General Licence GBOGE2009/01048. The files and the hardware are also subject to controls if exported.

The ADPe-XRC-4 is only supported for the FX140 variant; the FX100 variant is not supported for this XRM.

Please contact the factory for further information.

7 Pinout

7.1 Virtex 4 Boards

| Samtec pin no | Function | 4LX | 4SX | 4FX | ADPE4FX |
|---------------|-------------------|-----|-----|-----|---------|
| 1 | i_ser_dir | H28 | H28 | C27 | F35 |
| 3 | q_ser_dir | H27 | H27 | C28 | G35 |
| 4 | osc_enab | C32 | C32 | K28 | D34 |
| 5 | reset_oe_l | K27 | K27 | L29 | F36 |
| 6 | synth_sdi | N22 | N22 | J29 | E36 |
| 7 | synth_sync | J27 | J27 | K29 | G36 |
| 8 | synth_goe | N23 | N23 | H29 | D36 |
| 9 | synth_le | H30 | H30 | F28 | E34 |
| 11 | synth_sclk | H29 | H29 | E28 | F34 |
| 12 | ser_oe_l | J29 | J29 | E29 | E37 |
| 13 | extrig | E33 | E33 | H27 | J32 |
| 15 | extrig_dir | E32 | E32 | G27 | K32 |
| 18 | i_sck | K28 | K28 | J26 | J37 |
| 19 | i_reset_l | C34 | C34 | F30 | M31 |
| 20 | i_sdio | K29 | K29 | K26 | J36 |
| 21 | i_cs_l | G33 | G33 | C30 | K33 |
| 22 | q_cs_l | L31 | L31 | G26 | K34 |
| 23 | i_sdo | G32 | G32 | D30 | L33 |
| 24 | synth_dir | L30 | L30 | F26 | L34 |
| 25 | q_sdio | L34 | L34 | F31 | V25 |
| 26 | q_sdo | M32 | M32 | D26 | H37 |
| 27 | q_sck | L33 | L33 | G31 | W26 |
| 28 | q_reset_l | M33 | M33 | E26 | G37 |
| 38 | ext_debug_p | F33 | F33 | F25 | M35 |
| 40 | ext_debug_n | F34 | F34 | F24 | L35 |
| 61 | q_chan_data_n(12) | H34 | H34 | E24 | T31 |
| 62 | q_chan_data_n(13) | K33 | K33 | C32 | U30 |
| 63 | q_chan_data_p(12) | H33 | H33 | D24 | R31 |
| 64 | q_chan_data_p(13) | K32 | K32 | C33 | U31 |
| 65 | q_chan_data_n(10) | P27 | P27 | C23 | V29 |
| 66 | q_divrst_n | K34 | K34 | J32 | R36 |

Table 1 : Virtex 4 Board Pinout (continued on next page)

| Sartec pin no | Function | 4LX | 4SX | 4FX | ADPE4FX |
|---------------|-------------------|------|------|-----|---------|
| 67 | q_chan_data_p(10) | N27 | N27 | C24 | V30 |
| 68 | q_divrst_p | J34 | J34 | K32 | P36 |
| 69 | q_chan_data_n(9) | N30 | N30 | C34 | K36 |
| 70 | brd_type | V30 | AF30 | F35 | P35 |
| 71 | q_chan_data_p(9) | N29 | N29 | D34 | K37 |
| 73 | q_chan_data_n(8) | Y33 | AK32 | D37 | T36 |
| 74 | q_chan_data_p(11) | T23 | AA28 | F34 | W35 |
| 75 | q_chan_data_p(8) | Y32 | AK31 | E37 | U36 |
| 76 | q_chan_data_n(11) | U23 | AA29 | E34 | W34 |
| 77 | q_chan_data_p(6) | R26 | W24 | G36 | N37 |
| 79 | q_chan_data_n(6) | T26 | Y24 | F36 | M37 |
| 81 | q_chan_data_n(5) | R29 | AE34 | K34 | V33 |
| 82 | q_chan_data_p(7) | N32 | AC28 | J37 | W32 |
| 83 | q_chan_data_p(5) | P29 | AE33 | L34 | V34 |
| 84 | q_chan_data_n(7) | P32 | AB28 | J36 | Y33 |
| 85 | q_chan_data_n(4) | P31 | AC30 | M31 | P37 |
| 87 | q_chan_data_p(4) | P30 | AC29 | N30 | R37 |
| 89 | q_dck_p | P34 | AD34 | E32 | T30 |
| 91 | q_dck_n | R34 | AC34 | D32 | T29 |
| 97 | adckck_p | AF29 | AL24 | T35 | AE36 |
| 99 | adckck_n | AF30 | AL25 | T34 | AD36 |
| 101 | q_chan_data_n(3) | U33 | AH34 | M33 | Y26 |
| 102 | i_dck_p | AA25 | AM21 | V37 | AE32 |
| 103 | q_chan_data_p(3) | U32 | AJ34 | N33 | AA26 |
| 104 | i_dck_n | AA26 | AM22 | U37 | AD32 |
| 121 | q_chan_data_p(2) | V23 | AG30 | R32 | AA36 |
| 122 | q_chan_data_p(0) | W32 | AH32 | R31 | Y32 |
| 123 | q_chan_data_n(2) | V24 | AG31 | P32 | AB36 |
| 124 | q_chan_data_n(0) | V32 | AH33 | T31 | Y31 |
| 125 | q_chan_data_n(1) | V27 | AK34 | L35 | AA23 |
| 126 | q_chan_ovr_p | Y29 | AM32 | U33 | AB28 |
| 127 | q_chan_data_p(1) | W27 | AK33 | M35 | AB23 |
| 128 | q_chan_ovr_n | W29 | AM33 | U32 | AB27 |
| 129 | i_chan_data_p(10) | AB32 | AB22 | U31 | AA35 |
| 130 | i_divrst_p | AA33 | AL33 | V28 | AA31 |
| 131 | i_chan_data_n(10) | AB33 | AB23 | U30 | AB35 |

Table 1 : Virtex 4 Board Pinout (continued on next page)

| Sartec pin no | Function | 4LX | 4SX | 4FX | ADPE4FX |
|---------------|-------------------|------|------|------|---------|
| 132 | i_divrst_n | AA34 | AL34 | U28 | AA30 |
| 133 | i_chan_data_n(11) | AA31 | AL31 | V25 | AB25 |
| 134 | i_chan_data_n(12) | Y28 | AH30 | V29 | Y27 |
| 135 | i_chan_data_p(11) | AB31 | AM31 | W26 | AB26 |
| 136 | i_chan_data_p(12) | Y27 | AJ30 | V30 | AA28 |
| 137 | i_chan_data_p(9) | T29 | AG32 | W27 | AA29 |
| 138 | i_chan_data_n(13) | AH34 | AN27 | M37 | AE33 |
| 139 | i_chan_data_n(9) | T30 | AG33 | V27 | Y29 |
| 140 | i_chan_data_p(13) | AJ34 | AP27 | N37 | AF33 |
| 141 | i_chan_data_p(8) | AA23 | AP21 | K37 | AD35 |
| 143 | i_chan_data_n(8) | AA24 | AP22 | K36 | AD34 |
| 145 | i_chan_data_n(7) | AE34 | AL21 | P37 | AD37 |
| 147 | i_chan_data_p(7) | AE33 | AK21 | R37 | AE37 |
| 149 | i_chan_data_p(6) | AG32 | AK22 | V34 | AF36 |
| 151 | i_chan_data_n(6) | AG33 | AK23 | V33 | AG36 |
| 153 | i_chan_data_p(4) | AD27 | AP29 | W32 | AD31 |
| 155 | i_chan_data_n(4) | AC27 | AN29 | Y33 | AD30 |
| 157 | i_chan_data_n(5) | AD29 | AP26 | AA34 | AH37 |
| 159 | i_chan_data_p(5) | AE29 | AP25 | Y34 | AG37 |
| 161 | i_chan_data_p(3) | AC32 | AH28 | AA35 | AJ37 |
| 163 | i_chan_data_n(3) | AC33 | AH29 | AB35 | AK37 |
| 165 | i_chan_data_n(2) | AL34 | AM27 | Y31 | AM36 |
| 167 | i_chan_data_p(2) | AL33 | AM26 | Y32 | AL36 |
| 169 | i_chan_data_n(0) | AH33 | AG26 | Y26 | AJ34 |
| 171 | i_chan_data_p(0) | AH32 | AG25 | AA26 | AH34 |
| 173 | i_chan_data_n(1) | AM33 | AF24 | AB27 | AM35 |
| 175 | i_chan_data_p(1) | AM32 | AG23 | AB28 | AL35 |
| 177 | i_chan_ovr_n | AH30 | AM25 | Y29 | AN37 |
| 179 | i_chan_ovr_p | AJ30 | AN25 | AA29 | AM37 |

Table 1 : Virtex 4 Board Pinout

7.2 Virtex 5 Boards

| Samtec pin no | Function | 5LX | 5T1 | 5T2 | 5T2 |
|---------------|-------------------|------|------|------|------|
| 1 | i_ser_dirm | AL6 | AP14 | Y34 | H39 |
| 3 | q_ser_dirm | AL5 | AN14 | AA34 | H38 |
| 4 | osc_enab | AN5 | AB10 | K38 | G38 |
| 5 | reset_oe_l | AL4 | AM13 | W35 | F40 |
| 6 | synth_sdi | AP5 | AA8 | K40 | E39 |
| 7 | synth_sync | AM5 | AN13 | Y35 | F39 |
| 8 | synth_goe | AP4 | AA9 | K39 | E40 |
| 9 | synth_le | AM6 | AB8 | P37 | P37 |
| 11 | synth_sclk | AN7 | AC8 | R37 | R37 |
| 12 | ser_oe_l | AM8 | AM12 | T37 | P38 |
| 13 | exttrig | AN8 | AC9 | N38 | M39 |
| 15 | exttrig_dirm | AN9 | AC10 | P38 | N39 |
| 18 | i_sck | AN10 | AK11 | N39 | K40 |
| 19 | i_reset_l | AP6 | AD9 | G39 | J38 |
| 20 | i_sdio | AM11 | AJ11 | M39 | K39 |
| 21 | i_cs_l | AM17 | AK9 | E40 | U38 |
| 22 | q_cs_l | AP17 | AJ10 | W38 | W38 |
| 23 | i_sdo | AN17 | AK8 | E39 | T37 |
| 24 | synth_dirm | AP16 | AJ9 | V39 | V39 |
| 25 | q_sdio | AP12 | AE11 | F40 | AA36 |
| 26 | q_sdo | AM15 | AH9 | M38 | AA34 |
| 27 | q_sck | AP11 | AF11 | F39 | AA35 |
| 28 | q_reset_l | AM16 | AH10 | L39 | Y34 |
| 38 | ext_debug_p | AP9 | AD10 | H40 | H40 |
| 40 | ext_debug_n | AP10 | AD11 | J40 | J40 |
| 61 | q_chan_data_n(12) | AB10 | AB5 | N41 | J41 |
| 62 | q_chan_data_n(13) | AB7 | AD7 | AA37 | K42 |
| 63 | q_chan_data_p(12) | AB11 | AA5 | M42 | H41 |
| 64 | q_chan_data_p(13) | AB8 | AC7 | Y37 | J42 |
| 65 | q_chan_data_n(10) | AJ6 | AD5 | U41 | M41 |
| 66 | q_divrst_n | AD7 | Y7 | M41 | N41 |
| 67 | q_chan_data_p(10) | AJ7 | AD4 | T42 | L42 |
| 68 | q_divrst_p | AE7 | AA6 | L42 | M42 |
| 69 | q_chan_data_n(9) | AH7 | AE6 | R40 | P40 |

Table 2 : Virtex 5 Board Pinout (continued on next page)

| Sartec pin no | Function | 5LX | 5T1 | 5T2 | 5TZ |
|---------------|-------------------|------|-----|------|------|
| 70 | brd_type | AC9 | Y6 | J41 | Y40 |
| 71 | q_chan_data_p(9) | AG7 | AD6 | P41 | N40 |
| 73 | q_chan_data_n(8) | AH8 | AF6 | Y40 | AA39 |
| 74 | q_chan_data_p(11) | AC10 | W7 | V40 | Y37 |
| 75 | q_chan_data_p(8) | AG8 | AE7 | W40 | AA40 |
| 76 | q_chan_data_n(11) | AD10 | V7 | W41 | AA37 |
| 77 | q_chan_data_p(6) | AE9 | Y11 | U42 | P41 |
| 79 | q_chan_data_n(6) | AF9 | W11 | V41 | R40 |
| 81 | q_chan_data_n(5) | AK8 | AJ6 | Y42 | V41 |
| 82 | q_chan_data_p(7) | AG11 | V8 | AA40 | V40 |
| 83 | q_chan_data_p(5) | AK9 | AJ7 | W42 | U42 |
| 84 | q_chan_data_n(7) | AF11 | U8 | AA39 | W41 |
| 85 | q_chan_data_n(4) | AH10 | AK6 | AA41 | Y42 |
| 87 | q_chan_data_p(4) | AJ10 | AK7 | AA42 | W42 |
| 89 | q_dck_p | AE8 | AG5 | Y39 | Y39 |
| 91 | q_dck_n | AF8 | AF5 | Y38 | Y38 |
| 97 | adock_p | AA4 | K8 | AE40 | AE40 |
| 99 | adock_n | AB5 | K9 | AD40 | AD40 |
| 101 | q_chan_data_n(3) | W11 | E8 | AC39 | AB42 |
| 102 | i_dck_p | AG1 | T8 | AV40 | AV40 |
| 103 | q_chan_data_p(3) | Y11 | E9 | AC40 | AB41 |
| 104 | i_dck_n | AG2 | U7 | AU39 | AU39 |
| 121 | q_chan_data_p(2) | W10 | F10 | AJ42 | AE42 |
| 122 | q_chan_data_p(0) | V9 | G8 | AC41 | AF41 |
| 123 | q_chan_data_n(2) | V10 | G10 | AJ41 | AD41 |
| 124 | q_chan_data_n(0) | V8 | H8 | AD42 | AF42 |
| 125 | q_chan_data_n(1) | V5 | J11 | AT42 | AH41 |
| 126 | q_chan_ovr_p | Y7 | D12 | AB39 | AJ42 |
| 127 | q_chan_data_p(1) | W5 | K11 | AR42 | AG42 |
| 128 | q_chan_ovr_n | Y8 | C12 | AC38 | AJ41 |
| 129 | i_chan_data_p(10) | Y6 | H10 | AL41 | AH40 |
| 130 | i_divrst_p | AA6 | A13 | AE42 | AB37 |
| 131 | i_chan_data_n(10) | W6 | H9 | AK42 | AJ40 |
| 132 | i_divrst_n | AA5 | B12 | AD41 | AB38 |
| 133 | i_chan_data_n(11) | W4 | J9 | AU41 | AC38 |
| 134 | i_chan_data_n(12) | AC5 | C13 | AH41 | AC39 |

Table 2 : Virtex 5 Board Pinout (continued on next page)

| Sartec pin no | Function | 5LX | 5T1 | 5T2 | 5TZ |
|---------------|-------------------|-----|-----|------|------|
| 135 | i_chan_data_p(11) | Y4 | J10 | AT41 | AB39 |
| 136 | i_chan_data_p(12) | AB6 | B13 | AG42 | AC40 |
| 137 | i_chan_data_p(9) | AD5 | G11 | AM41 | AL41 |
| 138 | i_chan_data_n(13) | AE6 | E11 | AF42 | AN41 |
| 139 | i_chan_data_n(9) | AD6 | G12 | AN41 | AK42 |
| 140 | i_chan_data_p(13) | AF5 | F11 | AF41 | AM41 |
| 141 | i_chan_data_p(8) | AH4 | M10 | AU42 | AP42 |
| 143 | i_chan_data_n(8) | AJ4 | L9 | AV41 | AP41 |
| 145 | i_chan_data_n(7) | AJ5 | N9 | AP41 | AU41 |
| 147 | i_chan_data_p(7) | AK4 | N10 | AP42 | AT41 |
| 149 | i_chan_data_p(6) | V4 | M6 | AN39 | AB34 |
| 151 | i_chan_data_n(6) | V3 | M5 | AP38 | AC34 |
| 153 | i_chan_data_p(4) | Y3 | M7 | AT39 | AC36 |
| 155 | i_chan_data_n(4) | Y2 | L6 | AR39 | AD35 |
| 157 | i_chan_data_n(5) | AA1 | P6 | AF37 | AE38 |
| 159 | i_chan_data_p(5) | AB1 | P7 | AG37 | AE39 |
| 161 | i_chan_data_p(3) | AC2 | R6 | AM37 | AG37 |
| 163 | i_chan_data_n(3) | AD1 | T6 | AL37 | AF37 |
| 165 | i_chan_data_n(2) | AE1 | R8 | AD37 | AT40 |
| 167 | i_chan_data_p(2) | AF1 | R7 | AD36 | AR40 |
| 169 | i_chan_data_n(0) | AK3 | G5 | AB36 | AK39 |
| 171 | i_chan_data_p(0) | AK2 | H5 | AC35 | AJ38 |
| 173 | i_chan_data_n(1) | AM1 | T11 | AD35 | AM39 |
| 175 | i_chan_data_p(1) | AL1 | T10 | AC36 | AL39 |
| 177 | i_chan_ovr_n | AL3 | U10 | AC34 | AM38 |
| 179 | i_chan_ovr_p | AM2 | T9 | AB34 | AN38 |

Table 2 : Virtex 5 Board Pinout

7.3 Virtex 6 Boards

| Samtec pin no | Function | 6TL | 6T1 | 6TGE |
|---------------|-------------------|-----|-----|------|
| 1 | i_ser_dirn | N39 | N39 | N39 |
| 3 | q_ser_dirn | N38 | N38 | N38 |
| 4 | osc_enab | M38 | M38 | M38 |
| 5 | reset_oe_l | T36 | T36 | T36 |
| 6 | synth_sdi | P40 | P40 | P40 |
| 7 | synth_sync | U36 | U36 | U36 |
| 8 | synth_goe | P41 | P41 | P41 |
| 9 | synth_le | L40 | L40 | L40 |
| 11 | synth_sclk | L39 | L39 | L39 |
| 12 | ser_oe_l | L41 | L41 | L41 |
| 13 | exttrig | T35 | T35 | T35 |
| 15 | exttrig_dirn | T34 | T34 | T34 |
| 18 | i_sck | M41 | M41 | M41 |
| 19 | i_reset_l | P38 | P38 | P38 |
| 20 | i_sdio | M42 | M42 | M42 |
| 21 | i_cs_l | P37 | P37 | P37 |
| 22 | q_cs_l | T40 | T40 | T40 |
| 23 | i_sdo | N36 | N36 | N36 |
| 24 | synth_dirn | R40 | R40 | R40 |
| 25 | q_sdio | R38 | R38 | R38 |
| 26 | q_sdo | N40 | N40 | N40 |
| 27 | q_sck | T39 | T39 | T39 |
| 28 | q_reset_l | N41 | N41 | N41 |
| 38 | ext_debug_p | P36 | P36 | P36 |
| 40 | ext_debug_n | P35 | P35 | P35 |
| 61 | q_chan_data_n(12) | V39 | V39 | V39 |
| 62 | q_chan_data_n(13) | U34 | U34 | U34 |
| 63 | q_chan_data_p(12) | U39 | U39 | U39 |
| 64 | q_chan_data_p(13) | V34 | V34 | V34 |
| 65 | q_chan_data_n(10) | U38 | U38 | U38 |
| 66 | q_divrst_n | V35 | V35 | V35 |
| 67 | q_chan_data_p(10) | U37 | U37 | U37 |
| 68 | q_divrst_p | W35 | W35 | W35 |
| 69 | q_chan_data_n(9) | U33 | U33 | U33 |

Table 3 : Virtex 6 Board Pinout (continued on next page)

| Sartec pin no | Function | 6TL | 6T1 | 6TGE |
|---------------|-------------------|------|------|------|
| 70 | brd_type | W38 | W38 | W38 |
| 71 | q_chan_data_p(9) | U32 | U32 | U32 |
| 73 | q_chan_data_n(8) | U41 | U41 | U41 |
| 74 | q_chan_data_p(11) | V40 | V40 | V40 |
| 75 | q_chan_data_p(8) | U42 | U42 | U42 |
| 76 | q_chan_data_n(11) | W40 | W40 | W40 |
| 77 | q_chan_data_p(6) | V33 | V33 | V33 |
| 79 | q_chan_data_n(6) | W33 | W33 | W33 |
| 81 | q_chan_data_n(5) | Y39 | Y39 | Y39 |
| 82 | q_chan_data_p(7) | W42 | W42 | W42 |
| 83 | q_chan_data_p(5) | Y40 | Y40 | Y40 |
| 84 | q_chan_data_n(7) | Y42 | Y42 | Y42 |
| 85 | q_chan_data_n(4) | Y35 | Y35 | Y35 |
| 87 | q_chan_data_p(4) | AA35 | AA35 | AA35 |
| 89 | q_dck_p | W32 | W32 | W32 |
| 91 | q_dck_n | Y33 | Y33 | Y33 |
| 97 | adock_p | AD32 | AD32 | AD32 |
| 99 | adock_n | AE32 | AE32 | AE32 |
| 101 | q_chan_data_n(3) | AB36 | AB36 | AB36 |
| 102 | i_dck_p | AH34 | AH34 | AH34 |
| 103 | q_chan_data_p(3) | AC36 | AC36 | AC36 |
| 104 | i_dck_n | AJ35 | AJ35 | AJ35 |
| 121 | q_chan_data_p(2) | AC41 | AC41 | AC41 |
| 122 | q_chan_data_p(0) | AA42 | AA42 | AA42 |
| 123 | q_chan_data_n(2) | AD41 | AD41 | AD41 |
| 124 | q_chan_data_n(0) | AB42 | AB42 | AB42 |
| 125 | q_chan_data_n(1) | AC33 | AC33 | AC33 |
| 126 | q_chan_ovr_p | AB39 | AB39 | AB39 |
| 127 | q_chan_data_p(1) | AC34 | AC34 | AC34 |
| 128 | q_chan_ovr_n | AA40 | AA40 | AA40 |
| 129 | i_chan_data_p(10) | AD42 | AD42 | AD42 |
| 130 | i_divrst_p | AC40 | AC40 | AC40 |
| 131 | i_chan_data_n(10) | AE42 | AE42 | AE42 |
| 132 | i_divrst_n | AD40 | AD40 | AD40 |
| 133 | i_chan_data_n(11) | AD33 | AD33 | AD33 |
| 134 | i_chan_data_n(12) | AB41 | AB41 | AB41 |

Table 3 : Virtex 6 Board Pinout (continued on next page)

| Samtec pin no | Function | 6TL | 6T1 | 6TGE |
|---------------|-------------------|------|------|------|
| 135 | i_chan_data_p(11) | AE33 | AE33 | AE33 |
| 136 | i_chan_data_p(12) | AA41 | AA41 | AA41 |
| 137 | i_chan_data_p(9) | AF42 | AF42 | AF42 |
| 138 | i_chan_data_n(13) | AD38 | AD38 | AD38 |
| 139 | i_chan_data_n(9) | AF41 | AF41 | AF41 |
| 140 | i_chan_data_p(13) | AE38 | AE38 | AE38 |
| 141 | i_chan_data_p(8) | AB32 | AB32 | AB32 |
| 143 | i_chan_data_n(8) | AB33 | AB33 | AB33 |
| 145 | i_chan_data_n(7) | AE39 | AE39 | AE39 |
| 147 | i_chan_data_p(7) | AE40 | AE40 | AE40 |
| 149 | i_chan_data_p(6) | AK38 | AK38 | AK38 |
| 151 | i_chan_data_n(6) | AJ38 | AJ38 | AJ38 |
| 153 | i_chan_data_p(4) | AJ42 | AJ42 | AJ42 |
| 155 | i_chan_data_n(4) | AK42 | AK42 | AK42 |
| 157 | i_chan_data_n(5) | AG37 | AG37 | AG37 |
| 159 | i_chan_data_p(5) | AF37 | AF37 | AF37 |
| 161 | i_chan_data_p(3) | AK40 | AK40 | AK40 |
| 163 | i_chan_data_n(3) | AL40 | AL40 | AL40 |
| 165 | i_chan_data_n(2) | AF36 | AF36 | AF36 |
| 167 | i_chan_data_p(2) | AF35 | AF35 | AF35 |
| 169 | i_chan_data_n(0) | AJ40 | AJ40 | AJ40 |
| 171 | i_chan_data_p(0) | AH39 | AH39 | AH39 |
| 173 | i_chan_data_n(1) | AF34 | AF34 | AF34 |
| 175 | i_chan_data_p(1) | AG34 | AG34 | AG34 |
| 177 | i_chan_ovr_n | AG33 | AG33 | AG33 |
| 179 | i_chan_ovr_p | AF32 | AF32 | AF32 |

Table 3 : Virtex 6 Board Pinout

7.4 Kintex/Virtex 7 Boards

| Samtec pin no | Function | K7 | V7 |
|---------------|-------------------|-----|------|
| 1 | i_ser_dir | J12 | AE35 |
| 3 | q_ser_dir | J11 | AE34 |
| 4 | osc_enab | L12 | AC31 |
| 5 | reset_oe_l | J13 | Y33 |
| 6 | synth_sdi | K14 | AB31 |
| 7 | synth_sync | K13 | Y32 |
| 8 | synth_goe | J14 | AB32 |
| 9 | synth_le | H12 | AE33 |
| 11 | synth_sclk | H11 | AE32 |
| 12 | ser_oe_l | E14 | W40 |
| 13 | exttrig | E11 | AD35 |
| 15 | exttrig_dir | F11 | AC34 |
| 18 | i_sck | J16 | Y42 |
| 19 | i_reset_l | E13 | AF32 |
| 20 | i_sdio | H16 | AA42 |
| 21 | i_cs_l | B12 | AA32 |
| 22 | q_cs_l | A12 | AD30 |
| 23 | i_sdo | C12 | AA31 |
| 24 | synth_dir | A11 | AC30 |
| 25 | q_sdio | C11 | AB42 |
| 26 | q_sdo | L16 | Y39 |
| 27 | q_sck | D11 | AB41 |
| 28 | q_reset_l | K16 | AA39 |
| 38 | ext_debug_p | H14 | AD32 |
| 40 | ext_debug_n | G14 | AD33 |
| 61 | q_chan_data_n(12) | D18 | AD37 |
| 62 | q_chan_data_n(13) | L18 | AV41 |
| 63 | q_chan_data_p(12) | D17 | AD36 |
| 64 | q_chan_data_p(13) | L17 | AU41 |
| 65 | q_chan_data_n(10) | F17 | AA37 |
| 66 | q_divrst_n | H19 | AH36 |
| 67 | q_chan_data_p(10) | G17 | Y37 |
| 68 | q_divrst_p | J19 | AG36 |
| 69 | q_chan_data_n(9) | B17 | AG34 |

Table 4 : Kintex/Virtex 7 Boards Board Pinout (continued on next page)

| Samtec pin no | Function | K7 | V7 |
|---------------|-------------------|-----|------|
| 70 | brd_type | J18 | AW42 |
| 71 | q_chan_data_p(9) | C17 | AF34 |
| 73 | q_chan_data_n(8) | C16 | AB37 |
| 74 | q_chan_data_p(11) | H20 | AB36 |
| 75 | q_chan_data_p(8) | D16 | AT41 |
| 76 | q_chan_data_n(11) | G20 | AU42 |
| 77 | q_chan_data_p(6) | F21 | AF35 |
| 79 | q_chan_data_n(6) | E21 | AF36 |
| 81 | q_chan_data_n(5) | C21 | AC36 |
| 82 | q_chan_data_p(7) | E19 | AY42 |
| 83 | q_chan_data_p(5) | D21 | AC35 |
| 84 | q_chan_data_n(7) | D19 | BA42 |
| 85 | q_chan_data_n(4) | C22 | AF37 |
| 87 | q_chan_data_p(4) | D22 | AE37 |
| 89 | q_dck_p | F20 | AV40 |
| 91 | q_dck_n | E20 | AW40 |
| 97 | adock_p | C25 | AU38 |
| 99 | adock_n | B25 | AV38 |
| 101 | q_chan_data_n(3) | D24 | AP38 |
| 102 | i_dck_p | L25 | AD40 |
| 103 | q_chan_data_p(3) | E24 | AN38 |
| 104 | i_dck_n | K25 | AD41 |
| 121 | q_chan_data_p(2) | D29 | AP41 |
| 122 | q_chan_data_p(0) | C24 | AR38 |
| 123 | q_chan_data_n(2) | C30 | AP42 |
| 124 | q_chan_data_n(0) | B24 | AR39 |
| 125 | q_chan_data_n(1) | C26 | BB39 |
| 126 | q_chan_ovr_p | B27 | AW37 |
| 127 | q_chan_data_p(1) | D26 | BB38 |
| 128 | q_chan_ovr_n | A27 | AY37 |
| 129 | i_chan_data_p(10) | E28 | AR42 |
| 130 | i_divrst_p | A25 | AY39 |
| 131 | i_chan_data_n(10) | D28 | AT42 |
| 132 | i_divrst_n | A26 | AY40 |
| 133 | i_chan_data_n(11) | B29 | AT40 |
| 134 | i_chan_data_n(12) | A30 | AV39 |

Table 4 : Kintex/Virtex 7 Boards Board Pinout (continued on next page)

| Sartec pin no | Function | K7 | V7 |
|---------------|-------------------|-----|------|
| 135 | i_chan_data_p(11) | C29 | AT39 |
| 136 | i_chan_data_p(12) | B30 | AU39 |
| 137 | i_chan_data_p(9) | F26 | AF42 |
| 138 | i_chan_data_n(13) | A28 | AT37 |
| 139 | i_chan_data_n(9) | B28 | AN39 |
| 140 | i_chan_data_p(13) | E26 | AR37 |
| 141 | i_chan_data_p(8) | E29 | AN40 |
| 143 | i_chan_data_n(8) | E30 | AN41 |
| 145 | i_chan_data_n(7) | E25 | AR40 |
| 147 | i_chan_data_p(7) | F25 | AP40 |
| 149 | i_chan_data_p(6) | K26 | AB38 |
| 151 | i_chan_data_n(6) | J26 | AB39 |
| 153 | i_chan_data_p(4) | L26 | AJ40 |
| 155 | i_chan_data_n(4) | L27 | AJ41 |
| 157 | i_chan_data_n(5) | H29 | AE38 |
| 159 | i_chan_data_p(5) | J29 | AD38 |
| 161 | i_chan_data_p(3) | M28 | AH40 |
| 163 | i_chan_data_n(3) | L28 | AH41 |
| 165 | i_chan_data_n(2) | K30 | AH39 |
| 167 | i_chan_data_p(2) | L30 | AG39 |
| 169 | i_chan_data_n(0) | N30 | AK38 |
| 171 | i_chan_data_p(0) | N29 | AJ38 |
| 173 | i_chan_data_n(1) | M27 | AK40 |
| 175 | i_chan_data_p(1) | N27 | AL40 |
| 177 | i_chan_ovr_n | N25 | AC39 |
| 179 | i_chan_ovr_p | N26 | AC38 |

Table 4 : Kintex/Virtex 7 Boards Board Pinout

In the example code, analogue data is encoded in 2's complement format and data is left-aligned as a signed16 bit value, so that 0x7FFC (+32764) represents positive full scale and 0x8000 (-32768) represents negative full scale.

OVERRRANGE goes high when the signal input is outwith the valid ADC input range.

8 Board Layout

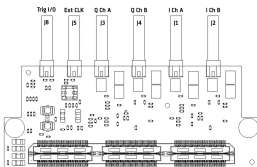


Figure 2 : I/O Layout

Revision History

| Date | Revision | Nature of Change |
|-----------|----------|---|
| Jul-2012 | 1.0 | First issue |
| Sept 2014 | 1.1 | Added references for Virtex7 and Kintex7 boards |
| Jan 2018 | 2.0 | converted to new document format |